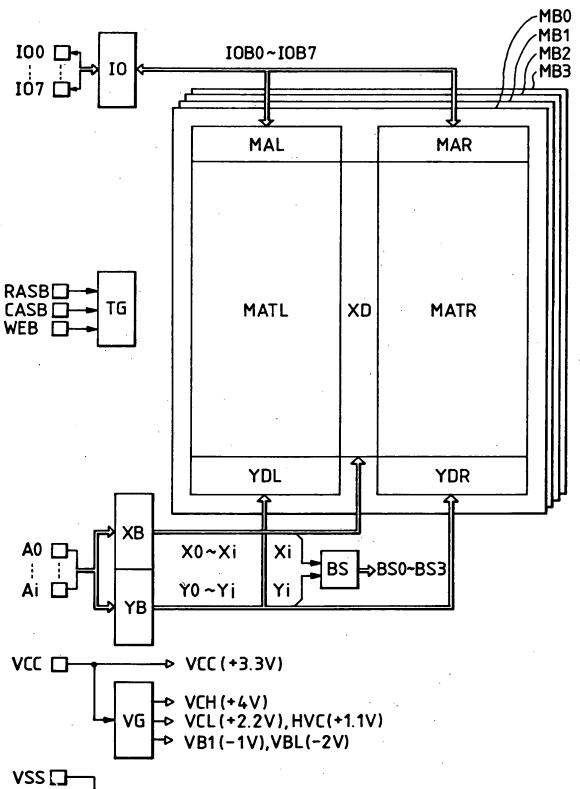
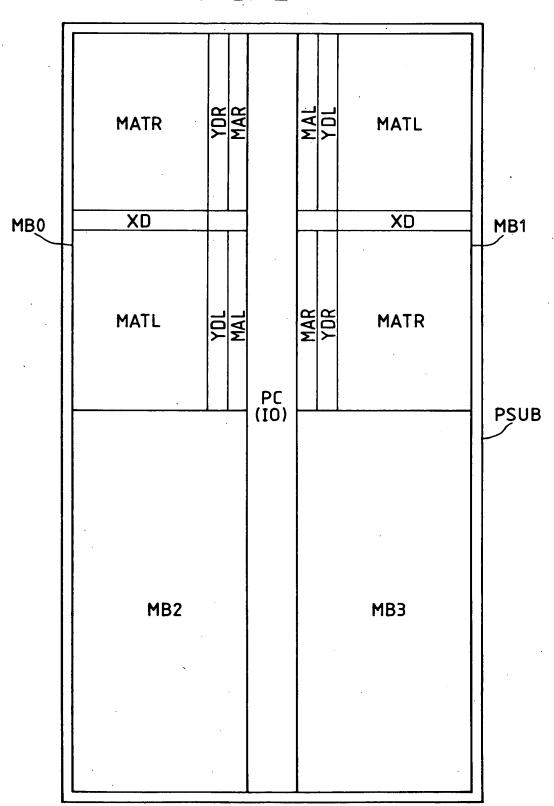
FIG. 1



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FIG. 2





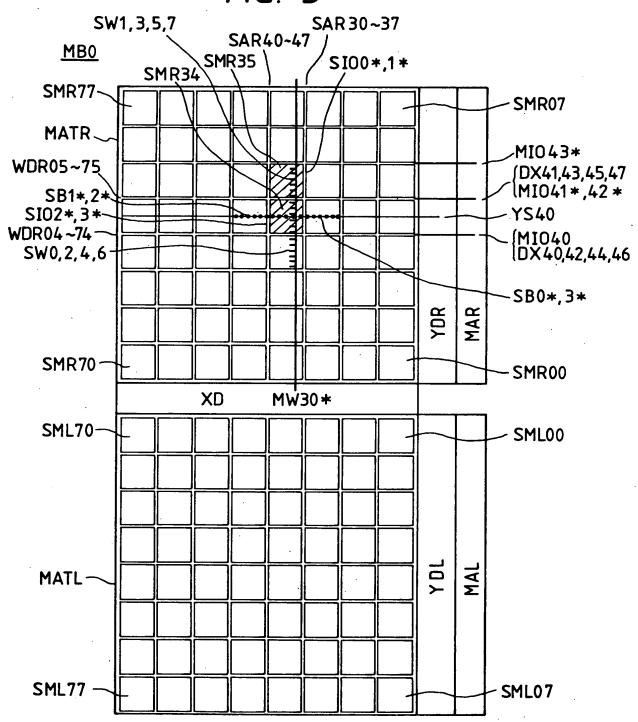


FIG. 4

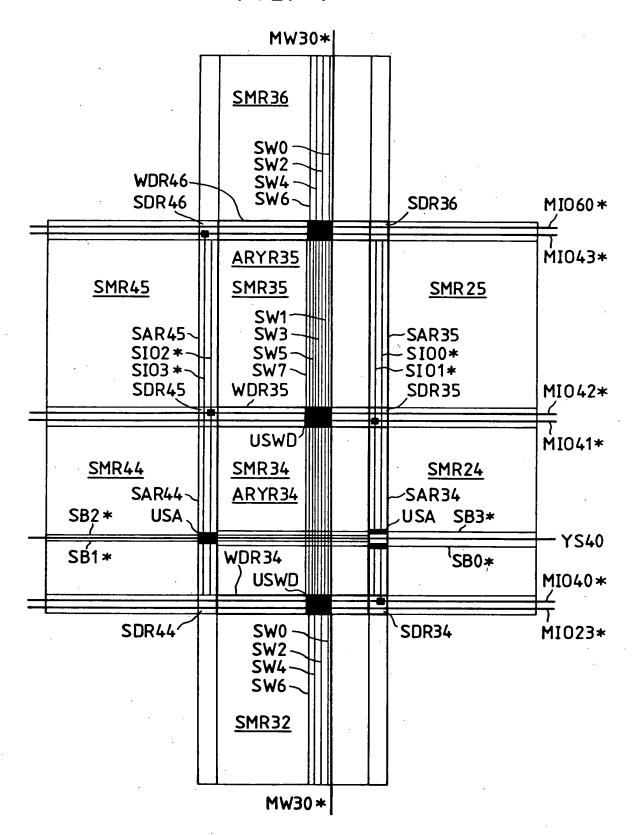
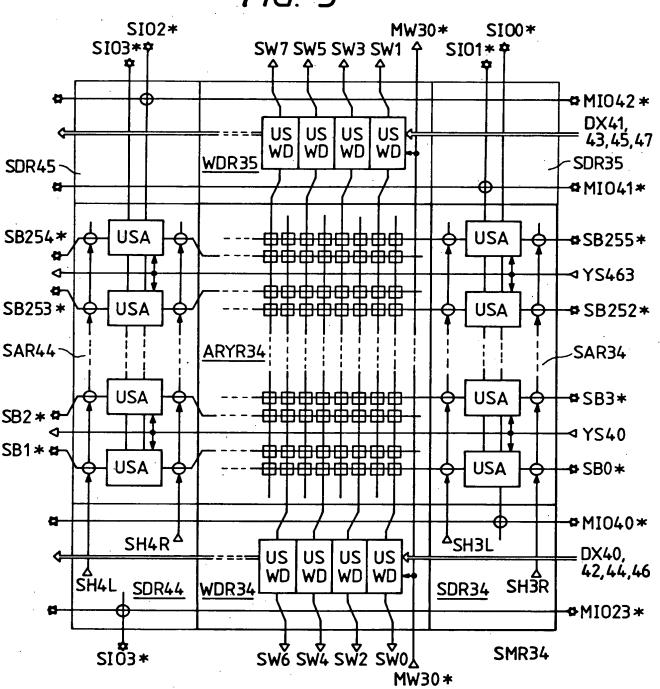


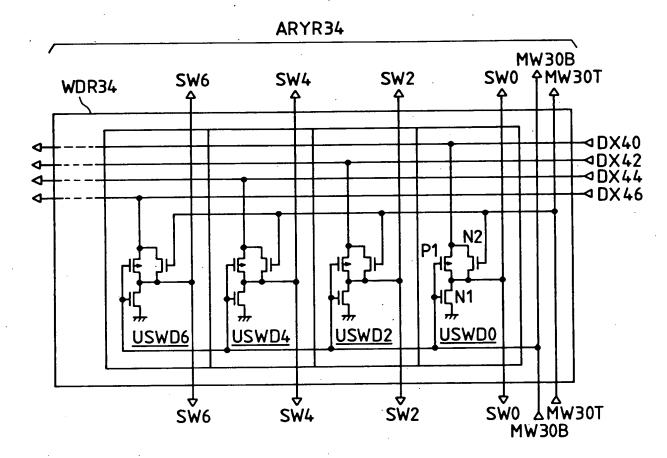
FIG. 5

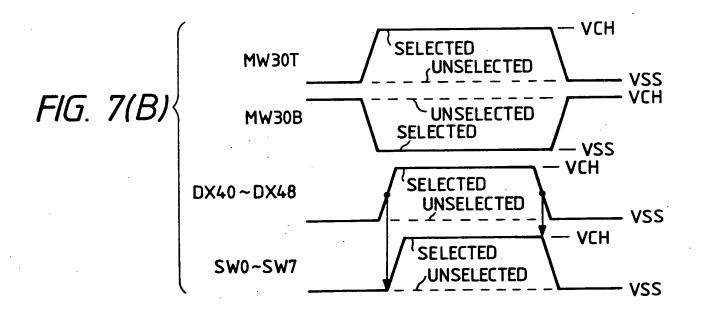


MEMORY CELL +, + SWITCH

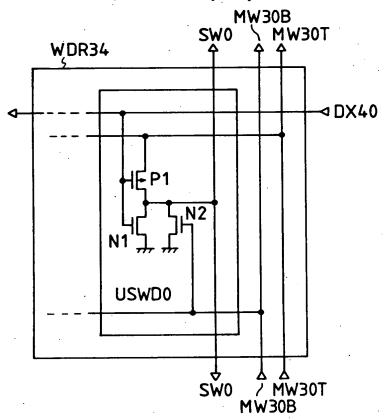
6/22 FIG. 6 US WD 5 US WD 3 US ¢ WD US & DX41,43,45,47 WD 7 WDR35 ARYR34 SW7 SW5 SW3 SW1 SAR44 SAR34 SB3T SB3T US **MM30*** А3 SB3B ◆ SB3B SB2T US **A2** SB2B **→** YS40 SB1T US **A1** SB1B NA NC SB0T SB0T US **MM30*** HVC⊳ **A0** SB0B^L NB ND **⇔**SB0B **SW6** SW4 SW2 SW₀ SH4R & SH3L SH4L SH3R US US US US WDR34 WD WD WD WD = DX40,42,44,46 6

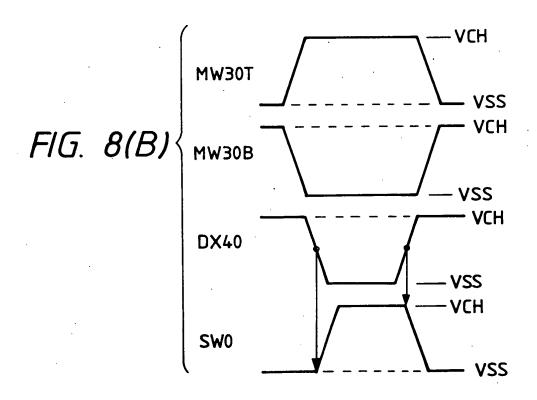
FIG. 7(A)



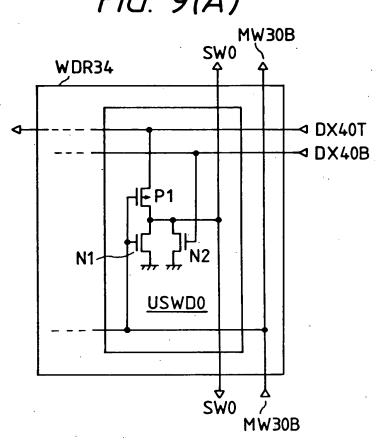


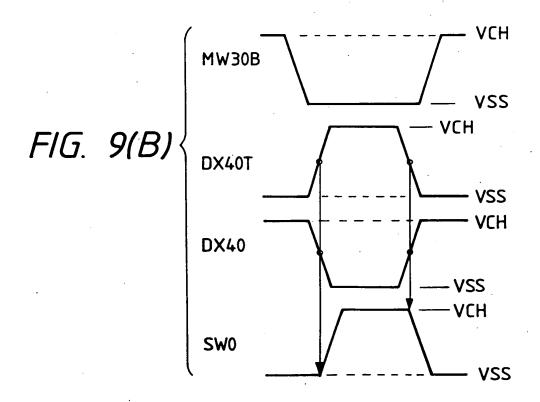
8/22 FIG. 8(A)

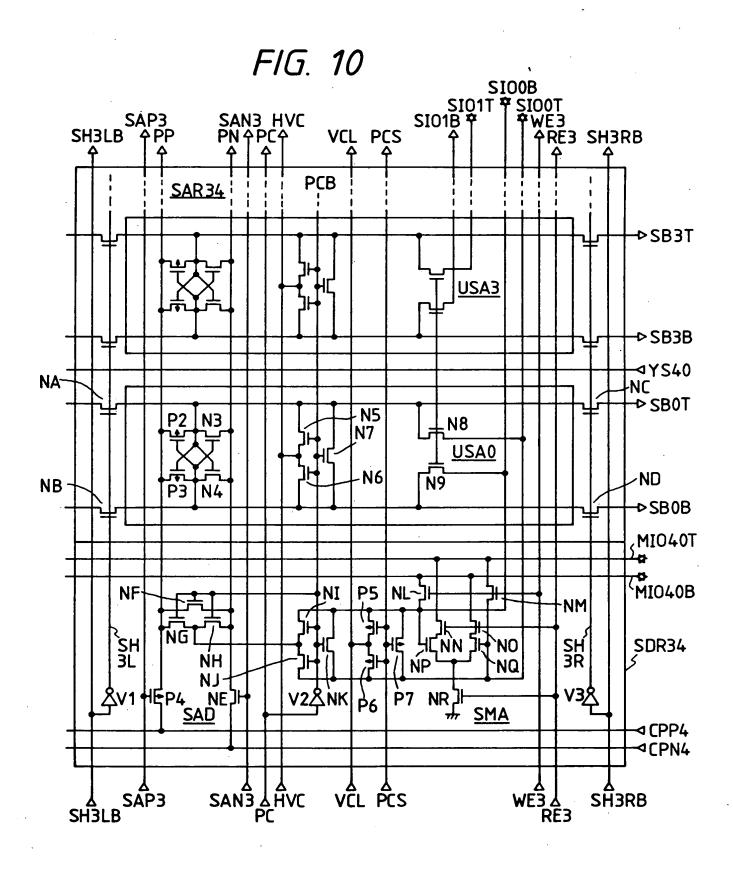


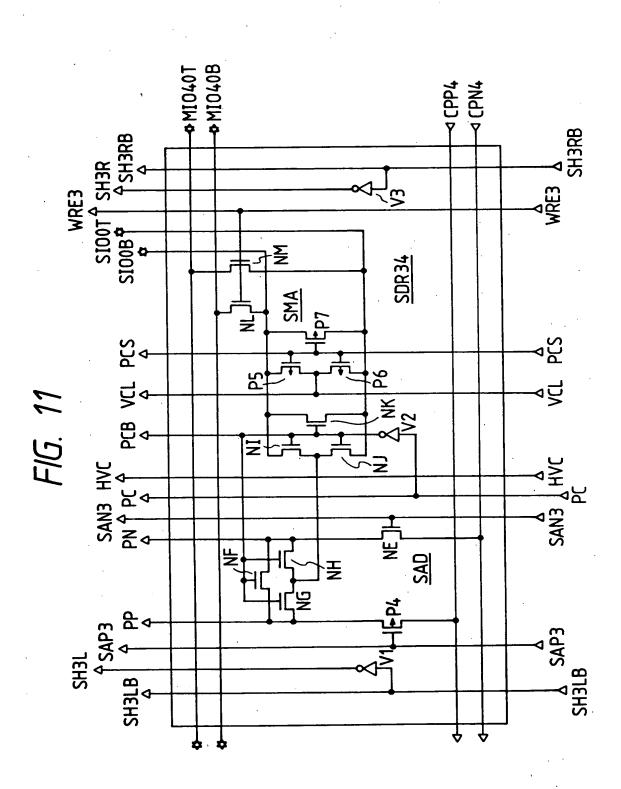


9/22 FIG. 9(A)









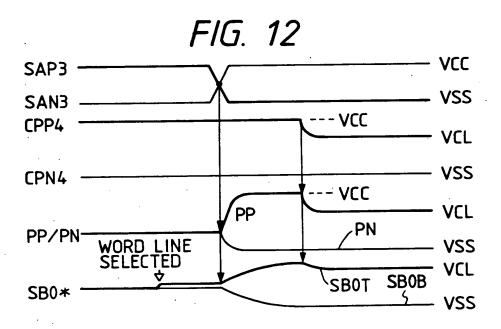
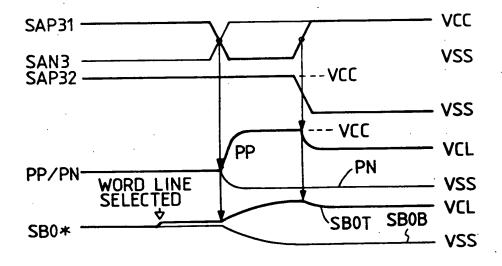


FIG. 14



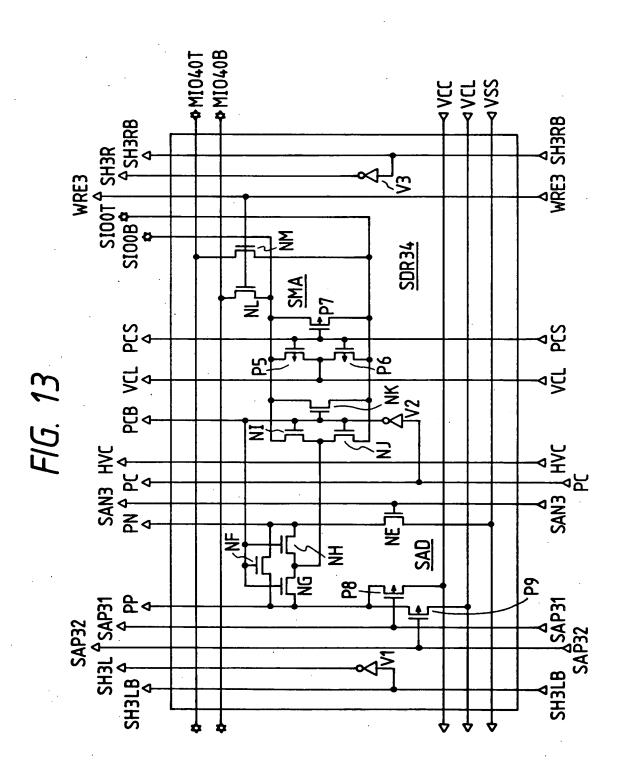


FIG. 15

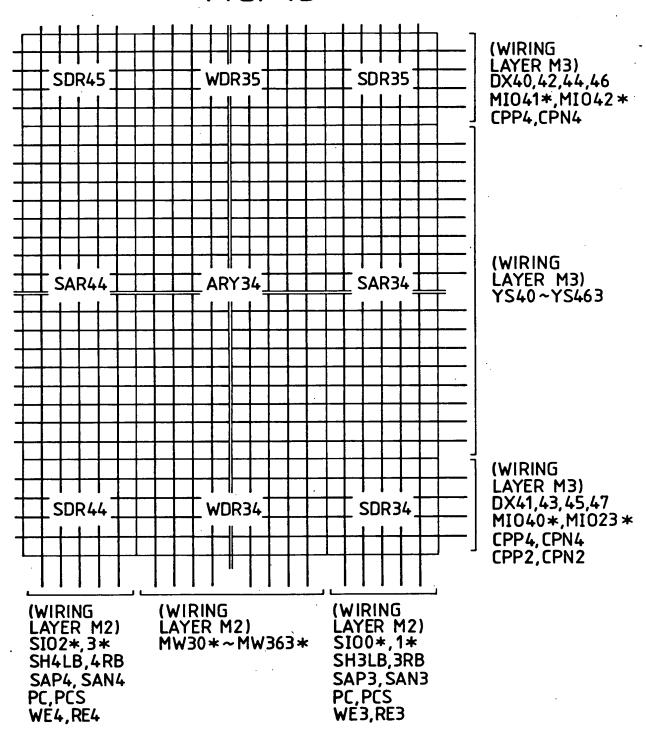


FIG. 16

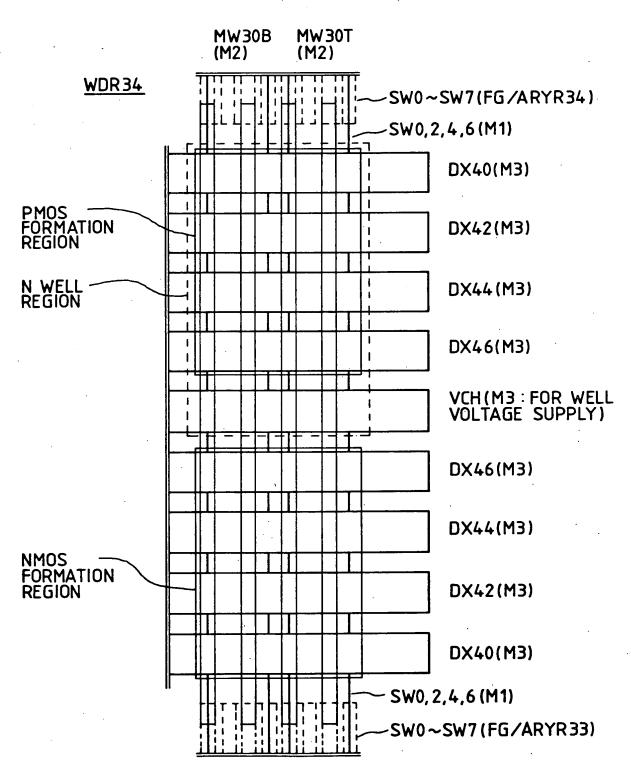
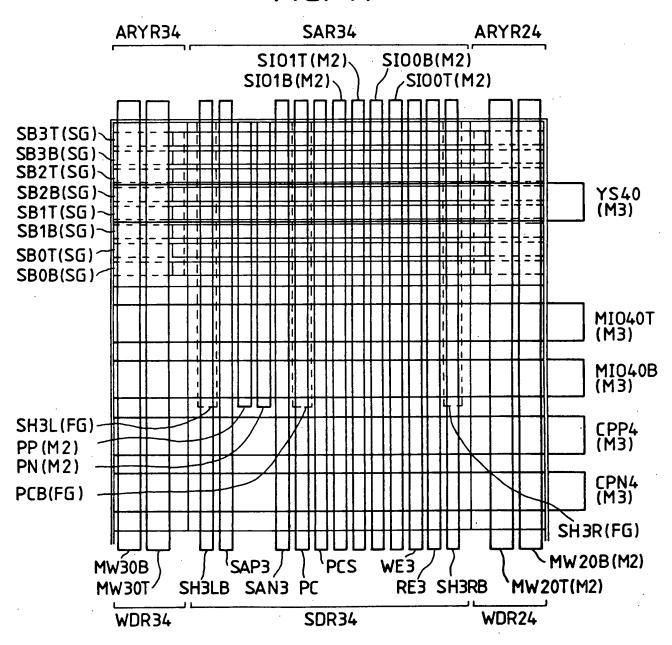
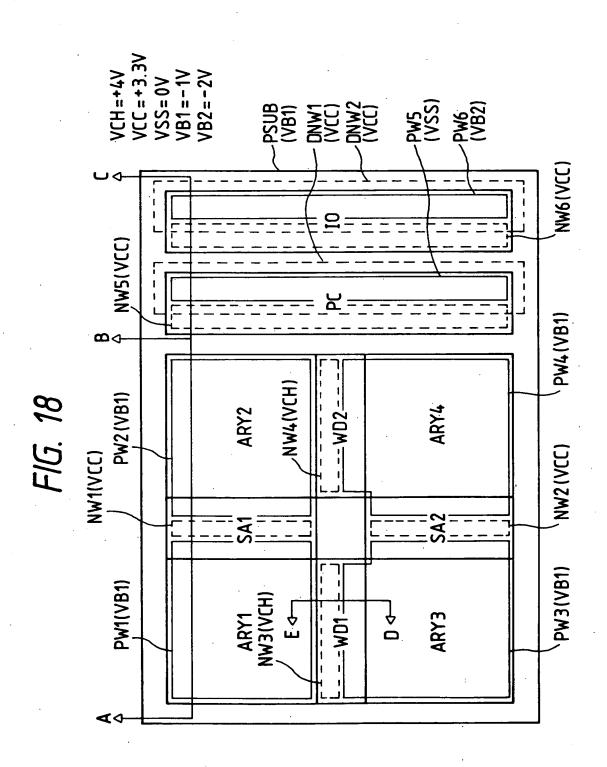
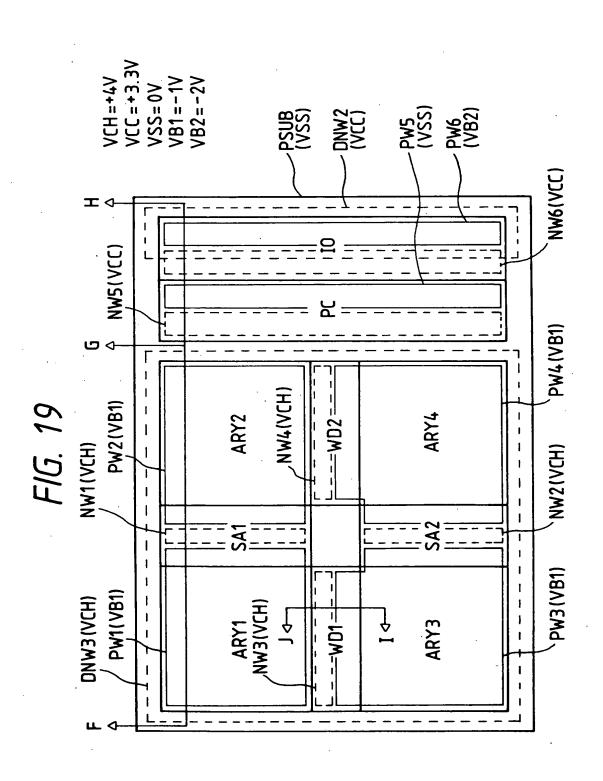


FIG. 17







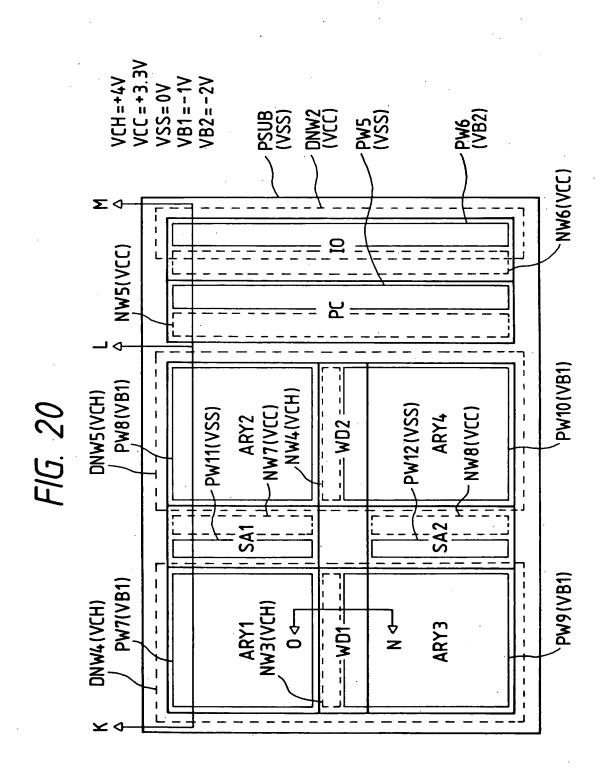


FIG. 21(A)

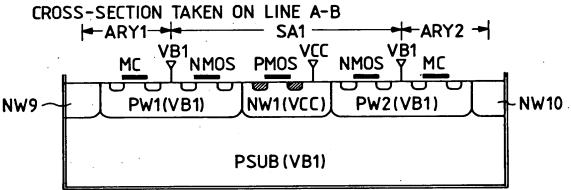


FIG. 21(B)

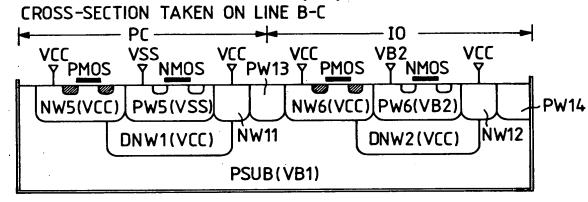
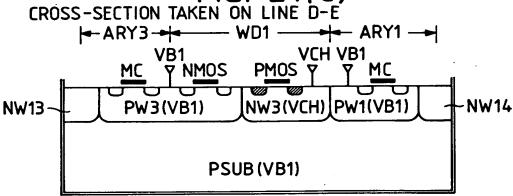


FIG. 21(C)

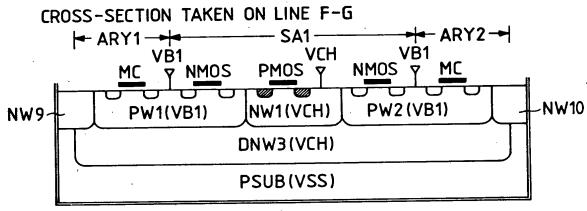


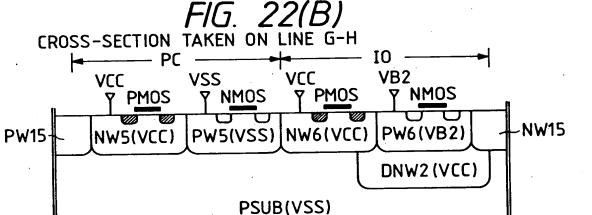
P* DIFFUSION : N* DIFFUSION LAYER LAYER

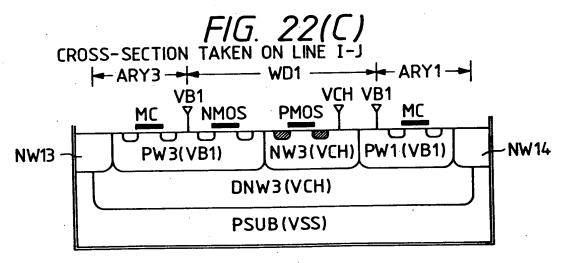
VCH=+4V VCC=+3.3V VSS=0V VB1=-1V VBB=-2V

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FIG. 22(A)



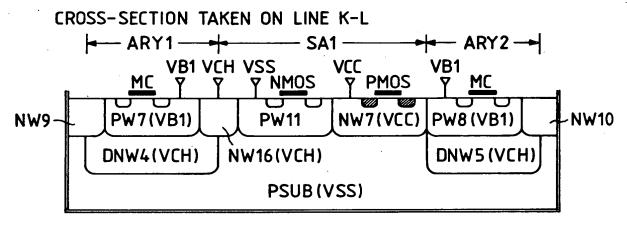


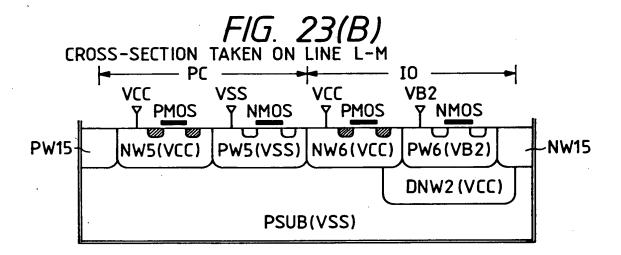


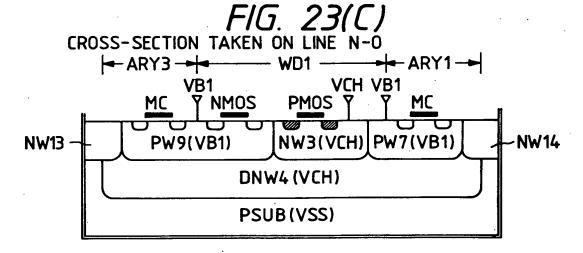
P* DIFFUSION :N* DIFFUSION
LAYER LAYER

VCH=+4V VCC=+3.3V VSS=0V VB1=-1V VBB=-2V

FIG. 23(A)







P* DIFFUSION :N* DIFFUSION
LAYER LAYER

VCH=+4V VCC=+3.3V VSS=0V VB1=-1V VBB=-2V